Amendment to the Specification

On page 7, following the paragraph that reads: "Figs. 16-99 are associated with the description below entitled 'Disclosure From Provisional Application 60/061,809,'" please insert the following text:

FIG. 16 is a diagram of fast-path and slow-path modes of communication processing.

FIG. 17 is a diagram of different buffers employed for the fast-path and slow-path modes of processing received messages.

FIG. 18 is a diagram of buffers employed for the fast-path and slow-path modes of transmitting messages.

FIG. 19 shows an initial format of an interrupt status register (ISR) of the present invention.

FIG. 20 is a table of register addresses of the present invention.

FIG. 21 shows mapping of network packets according to the present invention with mbufs and buffer descriptors.

FIG. 22 shows some control information structures used to represent network addresses and protocols according to the present invention.

FIG. 23 shows a host interface structure combining plural protocol stacks and drivers for working with an add-on INIC.

FIG. 24 shows a received TCP packet after processing by the INIC.

FIG. 25 shows a received ARP frame after processing by the INIC.

FIG. 26A shows a received data packet for a TCP fast-path connection.

FIG. 26B shows a received data packet for a TCP slow-path connection.

FIG. 26C shows a received ARP frame.

FIG. 27 shows sending a fast-path data packet.

FIG. 28 shows sending a slow-path data packet.

FIG. 29 shows sending a non-data command to the INIC.

FIG. 30 is a list of SRAM requirements for receive and transmit engines of the present invention.

FIG. 31 is a summary of a main loop of receive processing of the present invention.

FIG. 32 shows a format of a SMB header of the present invention.

FIG. 33 is a summary of a main loop of transmit processing of the present invention.

FIG. 34 shows the structure of a PCI address register of the present invention.

FIG. 35 shows a mapping of configuration space reads of the present invention.

FIG. 36 shows command fields for network and debug functions of the present invention.

FIG. 37 shows status fields for various functions of the present invention.

FIG. 38 is a diagram of INIC hardware of the present invention.

FIG. 39 shows an area on a die of various modules of the present invention

FIG. 40 shows a data path bandwidth of various channels of the present invention

FIG. 41 shows a CPU bandwidth of the present invention

FIG. 42 is a functional diagram of a communications microprocessor included in the INIC.

FIG. 43 is a list of instruction types of an instruction set for the communications microprocessor.

FIG. 44 is a "C-like" description of sequencer behavior.

FIG. 45 is a table of ALU operations.

FIG. 46 is a table of ALU operations.

FIG. 47 is a table of selected operands.

FIG. 48 is a table of selected operands.

FIG. 49 is a table of selected operands.

FIG. 50 is a diagram showing the relationship of FIG. 50A, FIG. 50B and FIG. 50C.

FIG. 50A is a table of selected operands.

FIG. 50B is a continuation of the table of FIG. 50A.

FIG. 50C is a continuation of the table of FIG. 50B.

FIG. 51 is a table of selected operands.

FIG. 52 is a table of selected tests.

FIG. 53 is a table of flag operations.

FIG. 54 is a diagram showing data flow between master and slave sequencers.

FIG. 55 shows data movement for a PCI slave write to DRAM.

FIG. 56 shows some major functions of an SRAM control sequencer.

FIG. 57 is a timing diagram of RAM accesses during a clock cycle.

FIG. 58 is a block diagram of an External Memory Control.

FIG. 59 is a block diagram of an External Memory Read Sequencer.

FIG. 60 is a timing diagram illustrating how data is read from SDRAM.

FIG. 61 is a block diagram of an External Memory Write Sequencer.

FIG. 62 is a timing diagram illustrating how data is written to SDRAM.

FIG. 63 is a block diagram of a PCI Master-Out Sequencer.

FIG. 64 is a block diagram of a PCI Master-In Sequencer.

FIG. 65 is a block diagram of a DRAM to PCI Sequencer.

FIG. 66 is a block diagram of a DRAM to PCI Sequencer.

FIG. 67 is a block diagram of a PCI to DRAM Sequencer.

FIG. 68 shows some major blocks involved in the movement of data from a PCI target to DRAM.

FIG. 69 is a block diagram of a SRAM to PCI Sequencer.

FIG. 70 shows some major blocks involved in the movement of data from SRAM to a PCI target.

FIG. 71 is a block diagram of a PCI to SRAM Sequencer.

FIG. 72 shows some major blocks involved in the movement of data from a PCI target to SRAM.

FIG. 73 is a block diagram of a DRAM to SRAM Sequencer.

FIG. 74 shows some major blocks involved in the movement of data from DRAM to SRAM.

FIG. 75 is a block diagram of a SRAM to DRAM Sequencer.

FIG. 76 shows some major blocks involved in the movement of data from SRAM to DRAM.

FIG. 77 shows a sequence of events when a PCI Slave Input Sequencer is the target of a PCI write operation.

FIG. 78 shows a sequence of events when a PCI Slave Input Sequencer is the target of a PCI read operation.

FIG. 79 is a block diagram of a Frame Receive Sequencer.

FIG. 80 shows a sequence of events including a successful reception of a packet.

FIG. 81 is a table illustrating a Receive Buffer Descriptor.

FIG. 82 is a table illustrating the offset and contents of a FreeClk at the completion of the frame receive operation.

FIG. 83 is a table illustrating the offset and contents of an IP and TCP header checksum.

FIG. 84 is a table illustrating a Receive Buffer Format.

FIG. 85 is a block diagram of a Frame Transmit Sequencer.

FIG. 86 shows a sequence of events including a successful transmission of a packet.

FIG. 87 is a table illustrating the offset and contents of a Transmit Buffer Descriptor.

FIG. 88 is a table illustrating a Transmit Buffer Format.

FIG. 89 is a table illustrating a Transmit Status Vector.

FIG. 90 is a block diagram shows some major functions of a Queue Manager.

FIG. 91 is a signal diagram showing the Queue Manager accepting operations from CPU and DMA sources.

FIG. 92 is a table illustrating some DMA Operations.

FIG. 93 is a table illustrating a format of aChannel Command Register.

FIG. 94 is a table illustrating a format of PCI to DRAM and PCI to SRAM Descriptors.

FIG. 95 is a table illustrating a format of DRAM to PCI and SRAM to PCI Descriptors.

FIG. 96 is a table illustrating a format of SRAM to DRAM, DRAM to DRAM and DRAM to SRAM Descriptors.

FIG. 97 is a table illustrating a format of an ending status of all channels.

FIG. 98 is a table illustrating a format of ChEvnt register.

FIG. 99 is a block diagram of a MAC Control.